are selectively connected with the word line, to apply the selection mirror voltage and reset mirror voltage to the memory cell.

7. The apparatus of claim **6**, wherein the snap-back event occurs when a voltage across the memory cell exceeds a threshold voltage, in response to the application of the selection mirror voltage to the word line.

8. The apparatus of claim **1**, wherein the NVRAM device comprises a cross-point memory array.

9. The apparatus of claim **1**, wherein the apparatus is disposed on an integrated circuit.

10. A method comprising:

applying a selection mirror voltage to a non-volatile random access memory (NVRAM) device, to select a memory cell of the NVRAM device; and

subsequent to applying the selection mirror voltage, applying a reset mirror voltage to the memory cell of the NVRAM device, to reset the memory cell,

wherein the reset mirror voltage is lower than the selection mirror voltage, to facilitate delivery of a reset current above a current threshold to the memory cell.

11. The method of claim **10**, wherein applying a selection mirror voltage includes applying voltage that is approximately equal to an inhibit voltage associated with the NVRAM device.

12. The method of claim **10**, wherein applying a selection mirror voltage to an NVRAM device includes:

coupling a selection mirror circuit with the NVRAM device; and

providing the selection mirror voltage, with the selection mirror circuit, to the NVRAM device.

13. The method of claim **10**, wherein applying a reset mirror voltage to the memory cell of the NVRAM device includes:

coupling a reset mirror circuit with the NVRAM device; and

providing the reset mirror voltage, with the reset mirror circuit, to the memory cell.

14. The method of claim **12**, wherein coupling a selection mirror circuit with the NVRAM device includes connecting the selection mirror circuit with a word line of the NVRAM device, wherein the memory cell is coupled with the word line.

15. The method of claim **14**, wherein coupling a reset mirror circuit with the NVRAM device includes connecting the reset mirror circuit with the word line of the NVRAM device.

16. The method of claim **10**, wherein applying a reset mirror voltage includes applying the reset mirror voltage after a snap-back event of the memory cell, wherein the snap-back event occurs in response to applying the selection mirror voltage to the NVRAM device, wherein the NVRAM device is a phase change memory (PCM) device.

17. A mobile device, comprising:

a processor; and

a memory coupled with the processor, wherein the memory includes:

a phase change memory (PCM) device;

a selection mirror circuit coupled with the PCM device to apply a selection mirror voltage to the PCM device, to select a memory cell of the PCM device; and

a reset mirror circuit coupled with the PCM device to apply a reset mirror voltage to the memory cell of the PCM device, subsequent to the application of the selection mirror voltage, to reset the memory cell,

wherein the reset mirror voltage is lower than the selection mirror voltage, to facilitate delivery of a reset current above a current threshold to the memory cell.

18. The mobile device of claim **17**, wherein the reset mirror circuit to apply a reset mirror voltage to the memory cell of the PCM device, subsequent to the application of the selection mirror voltage, includes to apply the reset mirror voltage after a snap-back event of the memory cell, wherein the snap-back event occurs in response to the application of the selection mirror voltage to the PCM device.

19. The mobile device of claim **18**, wherein the memory cell is coupled with a word line of the PCM memory device, and wherein the selection mirror circuit and reset mirror circuit are connectable with the word line, to apply the selection mirror voltage and reset mirror voltage to the memory cell.

20. The mobile device of claim **19**, wherein the snap event occurs when a voltage across the memory cell exceeds a threshold voltage, in response to the application of the selection mirror voltage to the word line.

21. The mobile device of claim **17**, wherein the selection mirror circuit to apply a selection mirror voltage includes to apply a voltage value that is approximately equal to an inhibit voltage associated with the PCM memory device.

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